

**800V N-Channel Power MOSFET**
**FEATURES**

- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

**APPLICATIONS**

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

Parameters Summary	
VDS: 800V	ID (at VGS=10V): 50A Rds(on) (at VGS=10V): 120mΩ (typ.)
	 SOT-227

**Device Ordering Marking Packing Information**

Ordering Number	Package	Marking	Packing
XBP50N80FX	SOT-227	XBP50N80FX	Tube


**Absolute Maximum Ratings**  $T_C = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ( $V_{GS} = 0\text{V}$ )	$V_{DSS}$	800	V
Continuous Drain Current	$I_D$	50	A
Pulsed Drain Current (note1)	$I_{DM}$	200	A
Gate-Source Voltage	$V_{GSS}$	$\pm 30$	V
Single Pulse Avalanche Energy (note2)	$E_{AS}$	4500	mJ
Repetitive Avalanche Energy (note1)	$E_{AR}$	60	mJ
Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	690	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55~+150	$^\circ\text{C}$

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

**Thermal Resistance**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.18	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	40	

Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	800	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 800V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1.0	$\mu A$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = 250\mu A$	2.5	--	4.5	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 25A$	--	120	130	m $\Omega$
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0\text{MHz}$	--	14600	--	pF
Output Capacitance	$C_{oss}$		--	1300	--	
Reverse Transfer Capacitance	$C_{rss}$		--	66	--	
Total Gate Charge	$Q_g$	$V_{DS} = 100V, I_D = 50A,$ $V_{GS} = 10V$	--	360	--	
Gate-Source Charge	$Q_{gs}$		--	20	--	
Gate-Drain Charge	$Q_{gd}$		--	120	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 100V, I_D = 50A,$ $R_G = 10\Omega$	--	110	--	ns
Turn-on Rise Time	$t_r$		--	200	--	
Turn-off Delay Time	$t_{d(off)}$		--	160	--	
Turn-off Fall Time	$t_f$		--	185	--	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	50	A
Pulsed Diode Forward Current	$I_{SM}$		--	--	400	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = 25A, V_{GS} = 0V$	--	--	1.4	V
Reverse Recovery Time	$t_{rr}$	$V_{GS} = 0V, I_S = 30mA,$ $di/dt = 100A/\mu s$	--	520	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	5.0	--	$\mu C$

**Notes**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $V_{DS} = 50V, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty Cycle  $\leq 1\%$

Figure 1. Maximum Transient Thermal Impedance

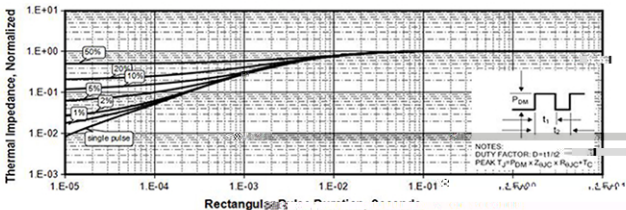


Figure 2. Maximum Power Dissipation vs Tc

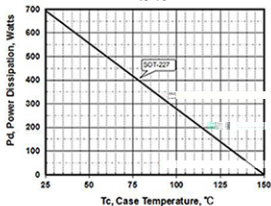


Figure 3. Maximum Continuous Drain Current vs Tc

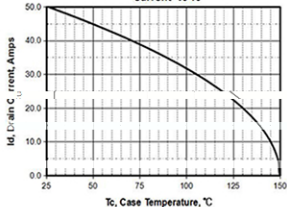


Figure 4. Output Characteristics

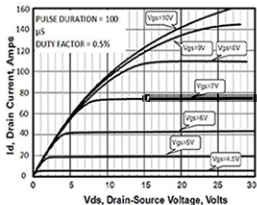


Figure 5.  $R_{ds(on)}$  vs Gate Voltage

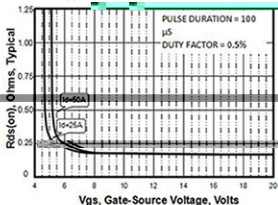


Figure 6. Peak Current Capability

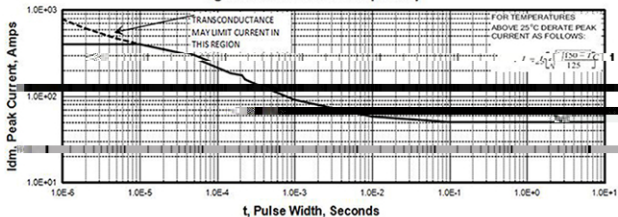


Figure 7. Transfer Characteristics

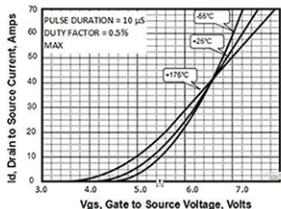


Figure 8. Unclamped Inductive Switching Capability

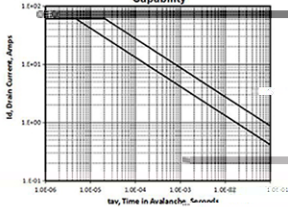


Figure 9.  $R_{DS(on)}$  vs Drain Current

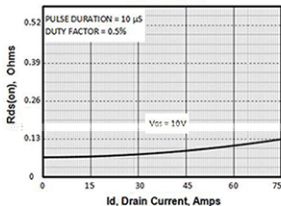


Figure 10.  $R_{DS(on)}$  vs Junction Temperature

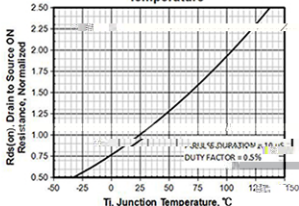


Figure 11. Breakdown Voltage vs Temperature

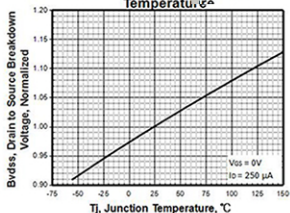


Figure 13. Maximum Safe Operating Area

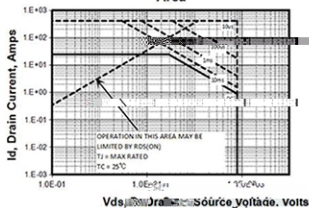


Figure 15. Typical Gate Charge

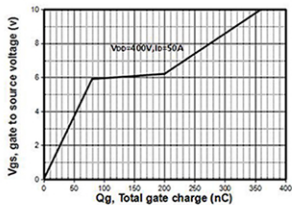


Figure 12. Threshold Voltage vs Temperature

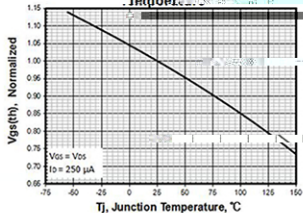


Figure 14. Capacitance vs Vds

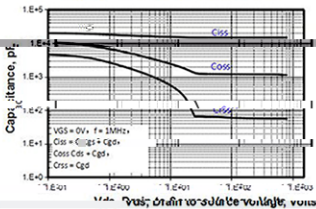
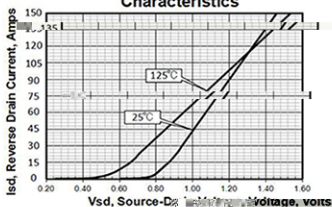


Figure 16. Body Diode Transfer Characteristics



## TEST CIRCUITS AND WAVEFORMS

Figure A: Gate Charge Test Circuit and Waveform

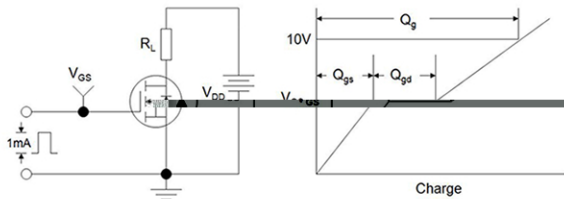


Figure B: Resistive Switching Test Circuit and Waveform

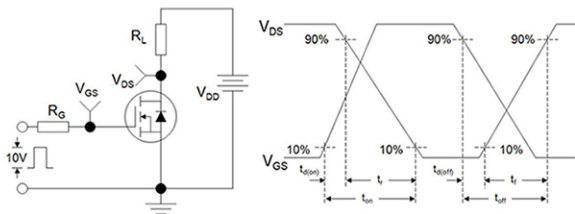


Figure C: Unclamped Inductive Switching Test Circuit and Waveform

